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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/560,703 | 12/13/2005 | Takefumi Nishimuta | 5000-5290 | 9339 |

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| EXAMINER | |
|---|---|
| SHINGLETON, MICHAEL B | |
| ART UNIT | PAPER NUMBER |
| 2815 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 01/03/2008 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTOPatentCommunications@Morganfinnegan.com
Shopkins@Morganfinnegan.com
jmedina@Morganfinnegan.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/560,703 | NISHIMUTA ET AL. | |
| | Examiner | Art Unit | |
| | Michael B. Shingleton | 2815 | |

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12-12-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

Figure 1 should and must be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Note that page 12 of the specification recites that this arrangement of Figure 1 is conventionally known. Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. US 6,754,478 (Lee) in view of Brunner et al. US 5,675,164 (Brunner).

Claims like claim 1 recites limitations like "A low noise amplifier with a MIS transistor, which amplifies an input signal suppressing the noise to a low level...", but the claimed details are solely directed to the so called "MIS transistor" structure and not to the circuitry of the amplifier itself in these claims. Thus, these claims are truly directed toward applicant's intention to use the specific MIS transistor structure somehow/somewhere in a low noise amplifier circuit and thus it appears that the patentability rests in the specifics of MIS transistor structure and not in the intended use of this transistor in a low noise amplifier circuit.

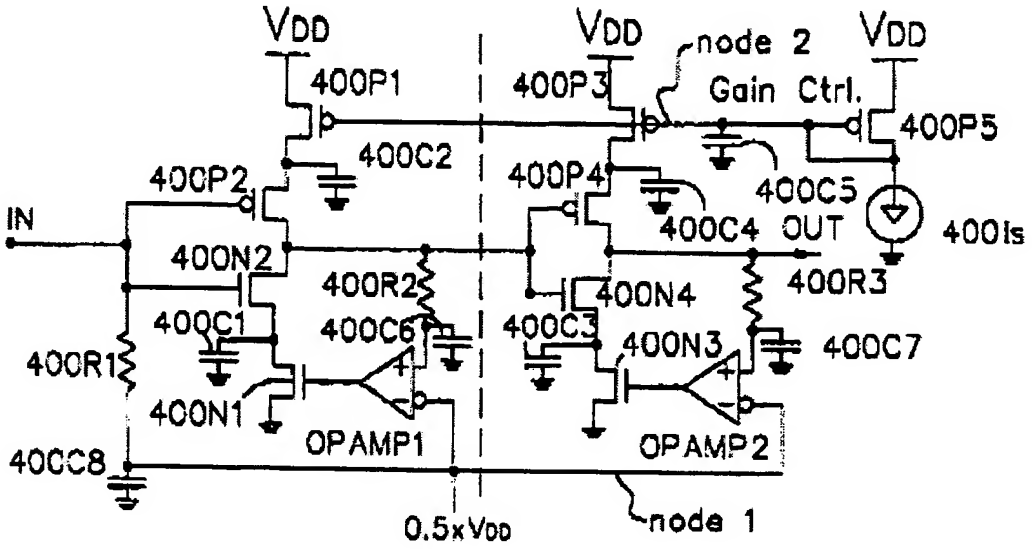


FIG. 4

Figure 4 of Lee.

Figure 4 of Lee discloses a low noise amplifier circuit having a CMOS (400P2, 400N2) and a feedback arrangement (OPAMP1, 400N1, 400C1) that is substantially identical to that of applicant's invention (See Figure 11 of applicant's invention.). Lee is silent on the exact construction of the MIS transistors that make up the CMOS arrangement. By being silent, this clearly indicates that any conventional MIS arrangement would work.

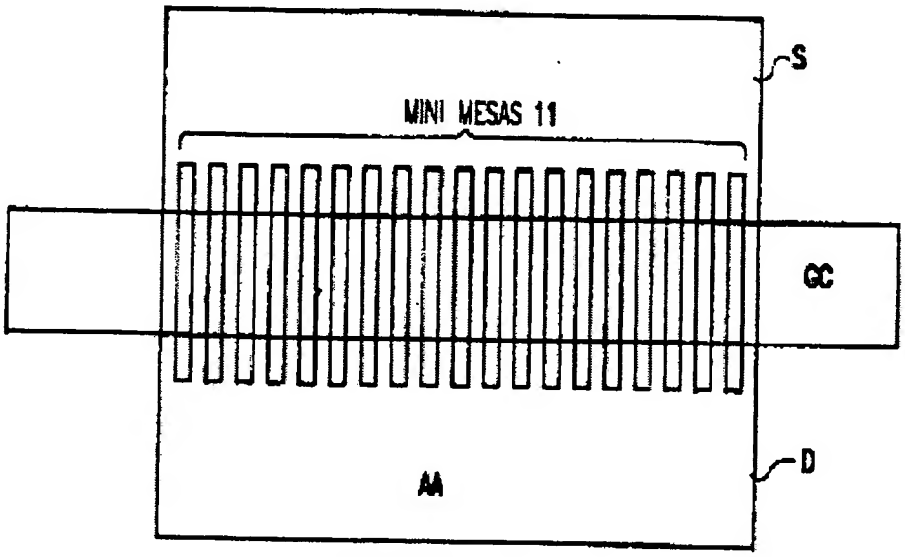


FIG.1

Figure 1 of Brunner.

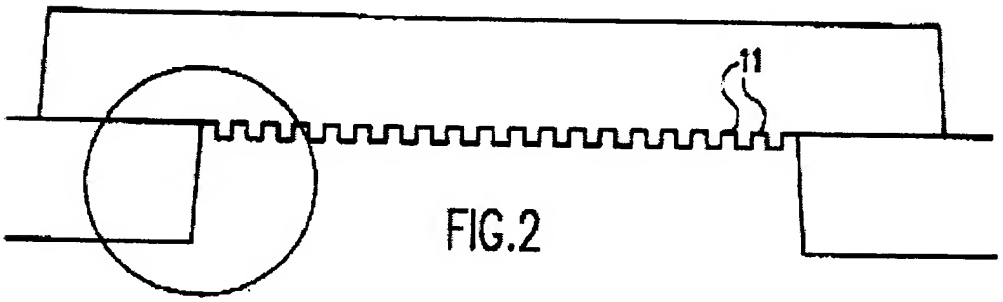


FIG.2

Figure 2 of Brunner.

Brunner discloses the specific structure of the MIS transistor as claimed. Of the Figures of Brunner to take note of, Figures 1, 2, 3 and 26 are the most relevant. Applicant should take note that the semiconductor substrate has at least one "fin" that is equivalent to the fin "810A" and "810B" of applicant's invention. Brunner utilizes the term "mesa" for these fins, but the term "fin" is also very common in the art for these transistor arrangements. Brunner is silent on each and every circuit that the transistor can be used in, but the fact is that transistors are meant to be used in circuits, otherwise transistors would not have utility.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the CMOS transistors with that of Brunner et al. because as the Lee reference is silent on the exact structure of the transistors that make up the amplifier circuit arrangement one of ordinary skill in the art would have been motivated to use any art-recognized equivalent transistor structure such as the one taught by Brunner.

Many of the claims include what is commonly referred to as product by process limitations. For example claim 4 recites that the gate insulator is "formed by...). These claims are limited to the structure claimed (See MPEP 2114) and while the claims are not specific on the specific insulator composition, the device of Brunner is seen as having this specific insulator composition and at the very least even if Brunner is not specific on the claimed composition of the insulator such an insulator composition is an art recognized equivalent to that of Brunner and accordingly it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the insulator of Brunner with the art recognized equivalent insulator as these are art recognized equivalents and are well known for their use as an insulator in semiconductor structures.

As to the crystal planes for the silicon substrate, Brunner is silent on the orientation of the substrate, thus any conventional orientation of the substrate would work and is included in the scope of the invention of Brunner. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide either a 100 plane, a 110 plane or a 111 plane for the substrate of Brunner because as the Brunner reference is silent on the exact orientation of the substrate one of ordinary skill in the art would have been motivated to use any conventional orientation such as those mentioned above. The silicon crystal of Brunner has to have an orientation and the ones claimed are merely common orientations for a silicon substrate used in semiconductor devices. These orientations fail to provide a patentable distinction over the prior art.

Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. US 6,754,478 (Lee) in view of Brunner et al. US 5,675,164 (Brunner) as applied to claims 1-12 above, and further in view of Applicant's admitted prior art AAPA.

Claims 13-15 recite that the low noise amplifier "is used in a direct conversion receiving system". Truly no further limiting structure is recited for the low noise amplifier. However, for examining purposes, the examiner is going to view these claims as a combination claim wherein the structure is that

of a direct conversion receiving system that includes a low noise amplifier having the specifically claimed MIS transistor structure.

AAPA discloses that the direct conversion receiving system is a conventional system and one part of that system employs a LNA or low noise amplifier.

One conventionally known art recognized equivalent amplifier system is that made obvious above.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the LNA of AAPA with that made obvious above because as the AAPA reference is silent on the exact structure or the LNA and is silent on which conventional LNA's if any can not be employed therefore one of ordinary skill in the art would have been motivated to use any art-recognized equivalent LNA such as the one made obvious above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker, can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
December 7, 2007

/Michael B Shingleton/
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Michael B Shingleton
Primary Examiner
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